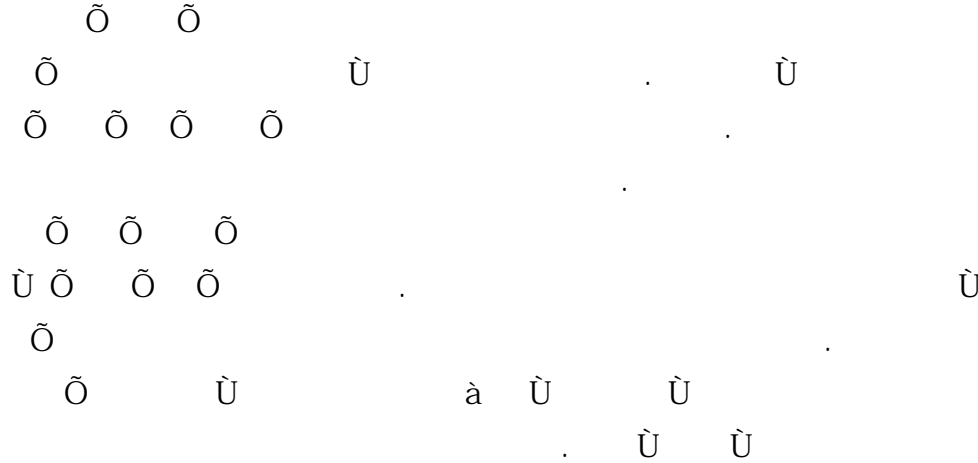


متحكم مؤسس على المعالج الدقيق
لتنظيم فولتية الخرج لمجهز القدرة غير المنقطع

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Microprocessor-Based Controller for the Uninterruptible Power Supply Voltage Regulation

By

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Abstract

Good regulation and stability are important factors to be considered in designing of the uninterruptible power supplies systems, which depend on the load requirements. On the other side, the cost factor roles the proper design selection of the uninterruptible power supply, especially for the commercial applications. A pulse width modulation uninterruptible power supplies are considered to have good features over the rival one.

This paper presents a suggested method for the controlling of the uninterruptible power supplies to regulate the output voltage, by using an easy practicable, low cost, and one-sensor, microprocessor-based regulator. This regulator circuit depends on minimizing the hardware complicity with efficient software. The practical results show that a good and reliable regulation performance in the applications when the fluctuation in both input DC voltage and load occurred, such as the applications using the solar cells or batteries as the input voltage source supplying variable load conditions.

(disturbance) (regulation) (UPS)

(switching conversion) ([1])

[2] (

on-) (PWM [3])

25 MHz (clock frequency) (DSP56001) DSP (line

(Lookup tables) [4]

5 (degree of freedom) (On-line) PWM

(inverters)

[5]

1. (load regulation) \emptyset

(1)

$$\text{Load reg} = \frac{V_{\text{out}}(\text{no-load}) - V_{\text{out}}(\text{full load})}{V_{\text{out}}(\text{no load})} * 100 \% \quad \dots(1)$$

2. (line regulation)

(2)

$$\text{Line reg} = \frac{V_{\text{out}}(\text{highest input}) - V_{\text{out}}(\text{lowest input})}{V_{\text{out}}(\text{nominal})} * 100 \% \quad \dots(2)$$

UPS

UPS (1) Intel 486 DX
 (Parallel .SIS 486 PCI/ISA(VER. C2) (mother board)
 ADC (Voltage Sensor) . PWM LPT1 Port)
 ADC AD573 10bit
 ADC (buffer)

16 .ISA slot ADC (2)
 ADC
 ADC (I/O memory) / 277H ADC
 16.8 usec 12 ADC st - conv
 18 end - conv ADC
 (4) ADC
 .ADC
 RD 74LS244
 (Bus)
 "0" st - conv .7474 D-Type Flip-Flop st - conv
 D₁₁ "1" ADC D₁₁
 (5)
 "0" st - conv (latched)
 "1" end - conv "1"
 ADC (MSB's)
 (3) 16-bit select LSByte
 " 0 " 16-bit select
 " 1 "

10bit ADC 19 20
 ISA-Slot -12V +5
 (voltage sensor) 14 UPS

ADC (10 Vp.p) .50 k ohm

ADC

10 bit ADC +5 -5 ADC (1)

\emptyset		ADC
V_{in}	0	512
$V_{in(max)}$	5	1023
$V_{in(min)}$	-5	0

ADC (1)

ADC

$$\Delta V = \frac{V_{in(max)} - V_{in(min)}}{2^{10} - 1} = 9.775 \text{ mV} \quad \dots (3)$$

1% UPS

$$\Delta reading(t) \approx \text{int}(.01V_{out} K_v \sin(\omega t) / \Delta V) \quad \dots(4)$$

(sensor gain) K_v

SIS 486 (VER. C2) (mother board)

Intel 486 DX

(off-line)

(PWM)

(lookup tables)

(fundamental)

N=12 (degree of freedom)

^[6]SLN1

PWM

50

(Normal binary (NB))

16-bit

%1

%100 %50

$\tilde{O} (\tilde{O} \tilde{U} \tilde{O} 51 \tilde{O}) \tilde{O} \tilde{O} \tilde{O} \tilde{O} . \tilde{O} \tilde{O} \tilde{O} \tilde{O} \tilde{U} \tilde{O} \tilde{O}$
 [51*50*2-byte=5100 byte] :

LPT1 (parallel Port)

\tilde{U} (driver circuit)
 (pin) "1"
 \tilde{U}
 "0" \tilde{U} (counter)
 (dead time)

UPS

\tilde{U}
 $\tilde{O} \tilde{U} \tilde{O}$ (sample)
 $\tilde{O} \tilde{U} \tilde{U} .$ (9) (6) $\tilde{U} \pi/2$
 $\tilde{O} \tilde{O} \tilde{U} \tilde{U} \tilde{U}$
 $\pi/2$ ADC $\tilde{O} \tilde{U}$
 $\tilde{O} \tilde{U} \tilde{U} \tilde{U}$
 $\tilde{O} \tilde{O} \tilde{O}$

.PWM \tilde{U}

$\tilde{O} \tilde{O} \tilde{O} \tilde{O} \tilde{U}$
 $\tilde{O} \tilde{O} \tilde{O} \tilde{U}$
 $\tilde{O} \tilde{O} \tilde{U} \tilde{U}$
 .PWM $\tilde{U} \tilde{U} \tilde{U}$

$\tilde{U} \tilde{O}$ \tilde{U}

$\tilde{O} \tilde{O} \tilde{O} \tilde{U}$
 $\tilde{O} \tilde{O} \tilde{O} \tilde{O}$

$\tilde{U} \tilde{U}$
 $\tilde{O} \tilde{U}$

$\tilde{U} \tilde{U}$ PWM
 $\tilde{O} \tilde{O} \tilde{U} \tilde{U}$ ADC \tilde{O}

(actuated) (proportional control)
 \tilde{O} value)
 $\tilde{U} \tilde{O}$ \tilde{U}

ADC : (4) .01

$$\Delta reading = \text{int}\left(\frac{.01 * (1/3.5) * 17.5 \sin(2\pi 50 * .0042)}{9.775m}\right) \cong 5 readings \dots(5)$$

int(difference between readings/5)

[4]8086

MOSFET (on-line) - UPS ((10))

.IRFP150 (smooth) 6.8uF

.IRFP150 MOSFET (11)

(buffer) 3507j (operational amplifier)

74LS244 PWM (source) 3601 (optocoupler)

(buffer) 3507j (operational amplifier)

MOSFET 10V

0.45 usec (fall time) 0.65 usec (rise time)

4usec (dead time)

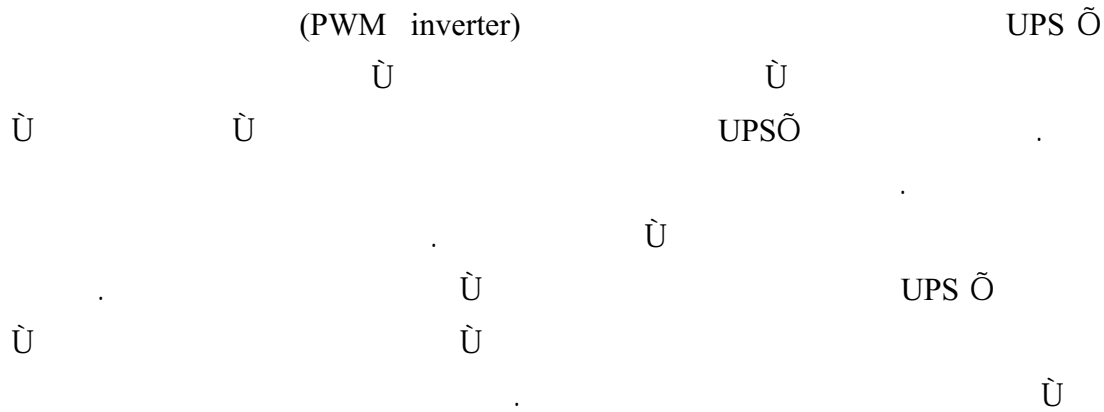
(13) (12)

(15) (14)

90%

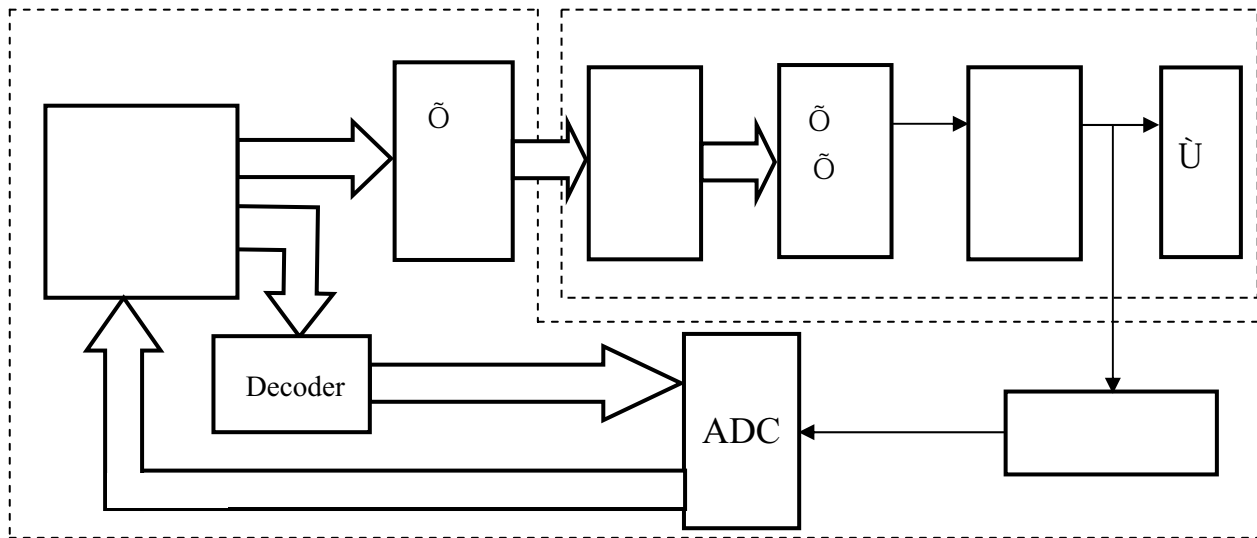
UPS PWM

.R=6.9 Ω V_d=10

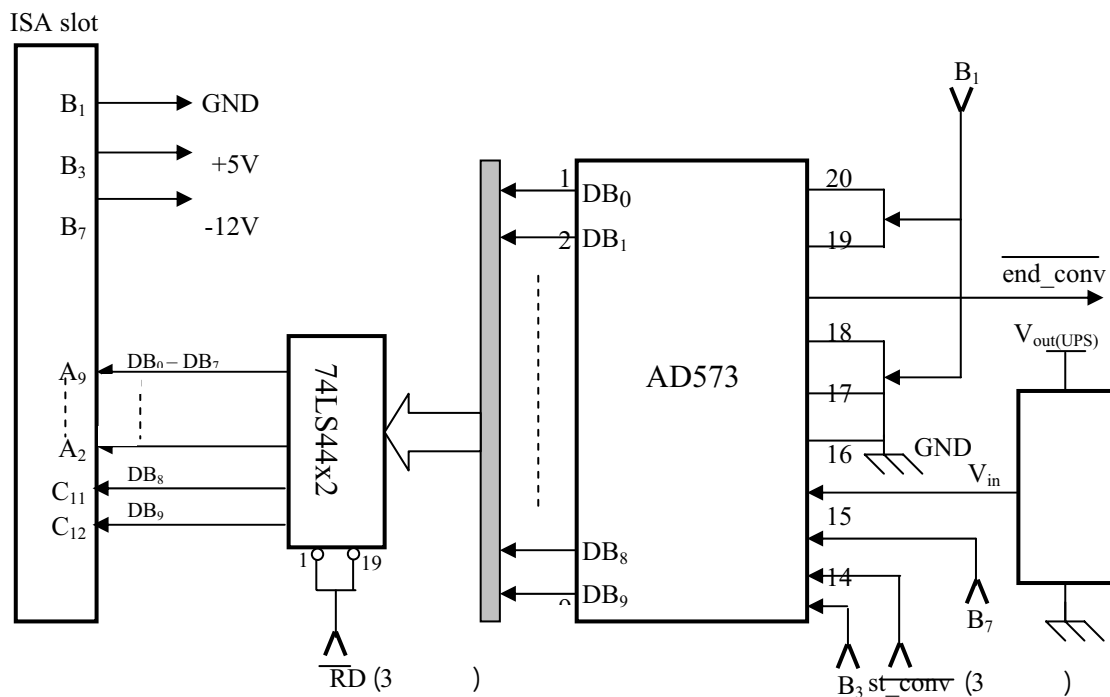


(References)

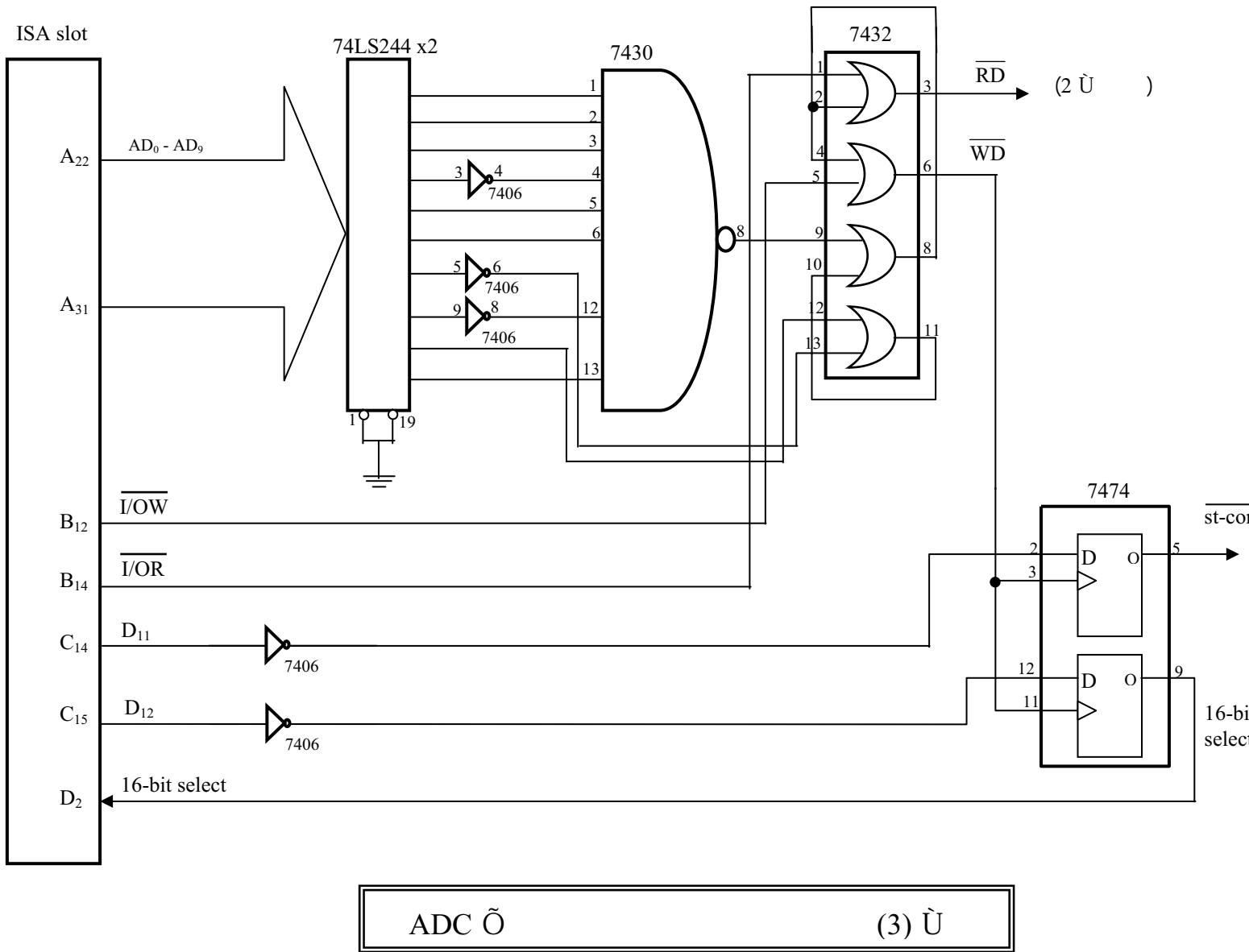
1. Kalyan P. Gokhale, Atsuo Kawamura & Richard G. Hoft. "Dead Beat Microprocessor Control of PWM Inverter for Sinusoidal Output Waveform Synthesis". IEEE Transactions. On Industry Applications, Vol. IA-23, No. 5, September/October 1987, pp. 901-910.
2. Philip T. Krein. "Elements of Power Electronics". Oxford University Press, Inc., New York, 1998.
3. Jian Sun, Stephan Beineke & Horst Grotstollen. "Optimal PWM Based on Real-Time Solution of Harmonic Elimination Equations". IEEE Transactions on Power Electronics, Vol. 11, No. 4, July 1996, pp. 612-621.
4. Barry b. Brey, "the 8086/8088 microprocessor architecture, programming and interfacing", Merrill publishing company, 1987.
5. Basil M. Saied, M. Khaled Shakfa. "Analytical Study Of UPS Regulator System Using Variable Structure Control (Arabic)", Al-Rafidain Engineering Journal, Vol. 11, No. 2, 2003, pp. 1-14.
6. Prasad N. Enjeti, Phoivos D. Ziogas, & James F. Lindsay. "Programmed PWM Techniques to Eliminate Harmonics: A Critical Evaluation". IEEE Transactions on Industry Applications, Vol. 26, No. 2, March/April 1990, pp. 302-316.

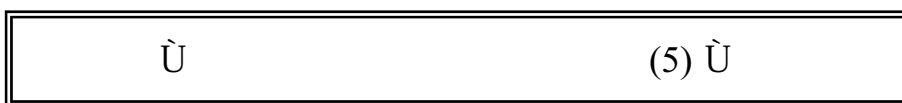
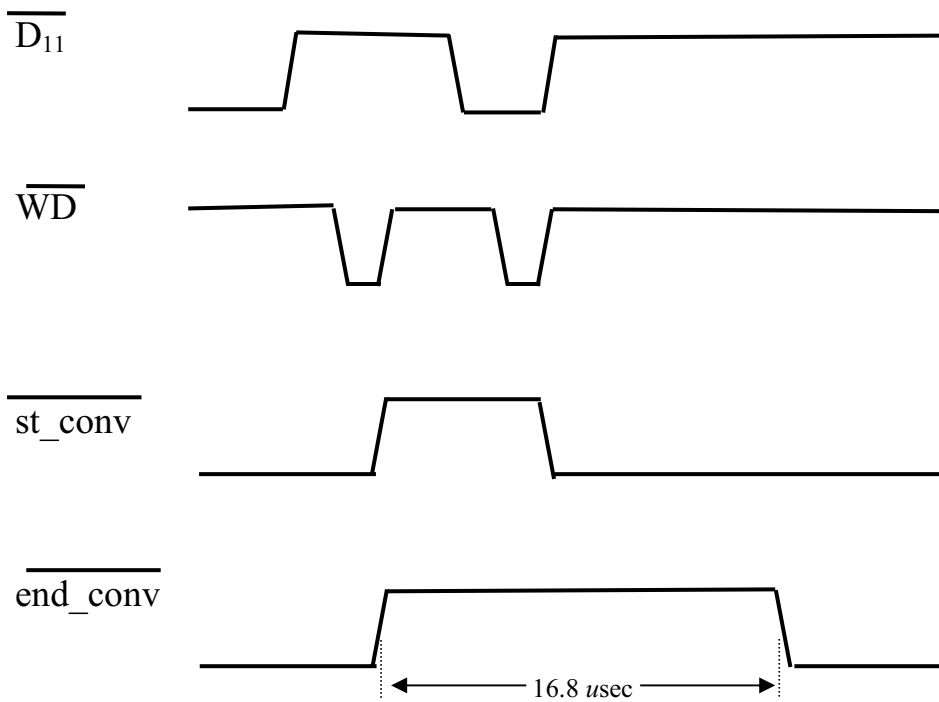
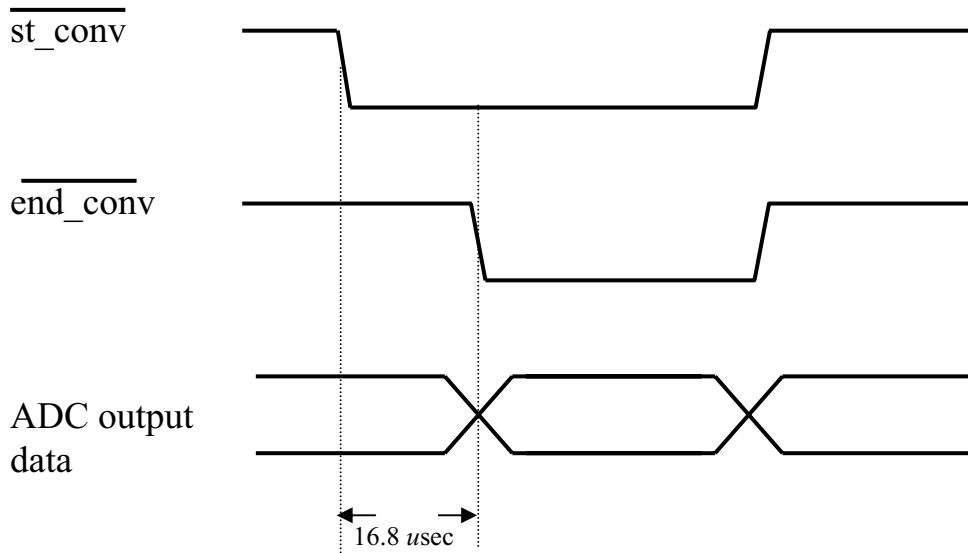


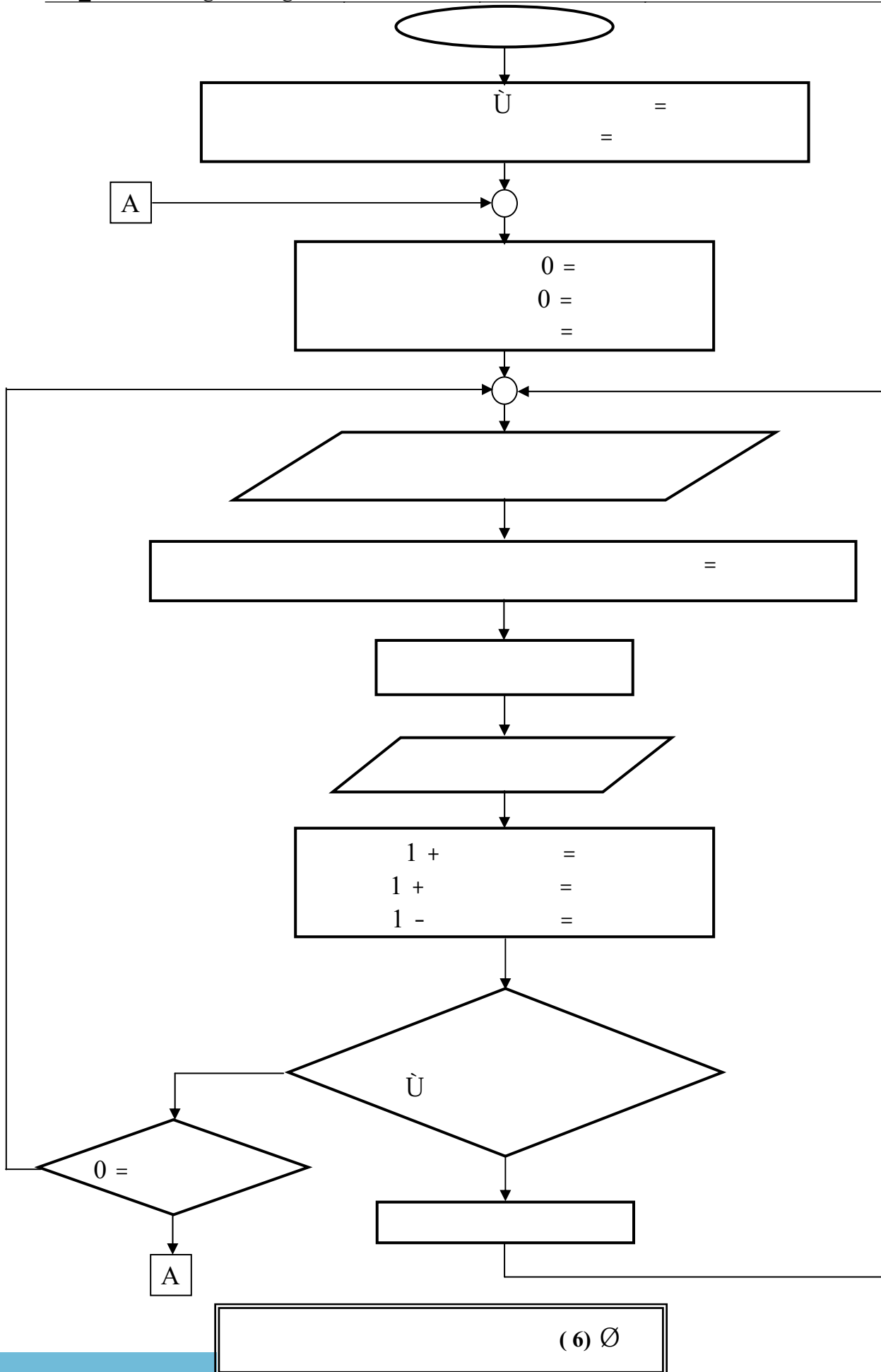
UPS Õ (1) Û

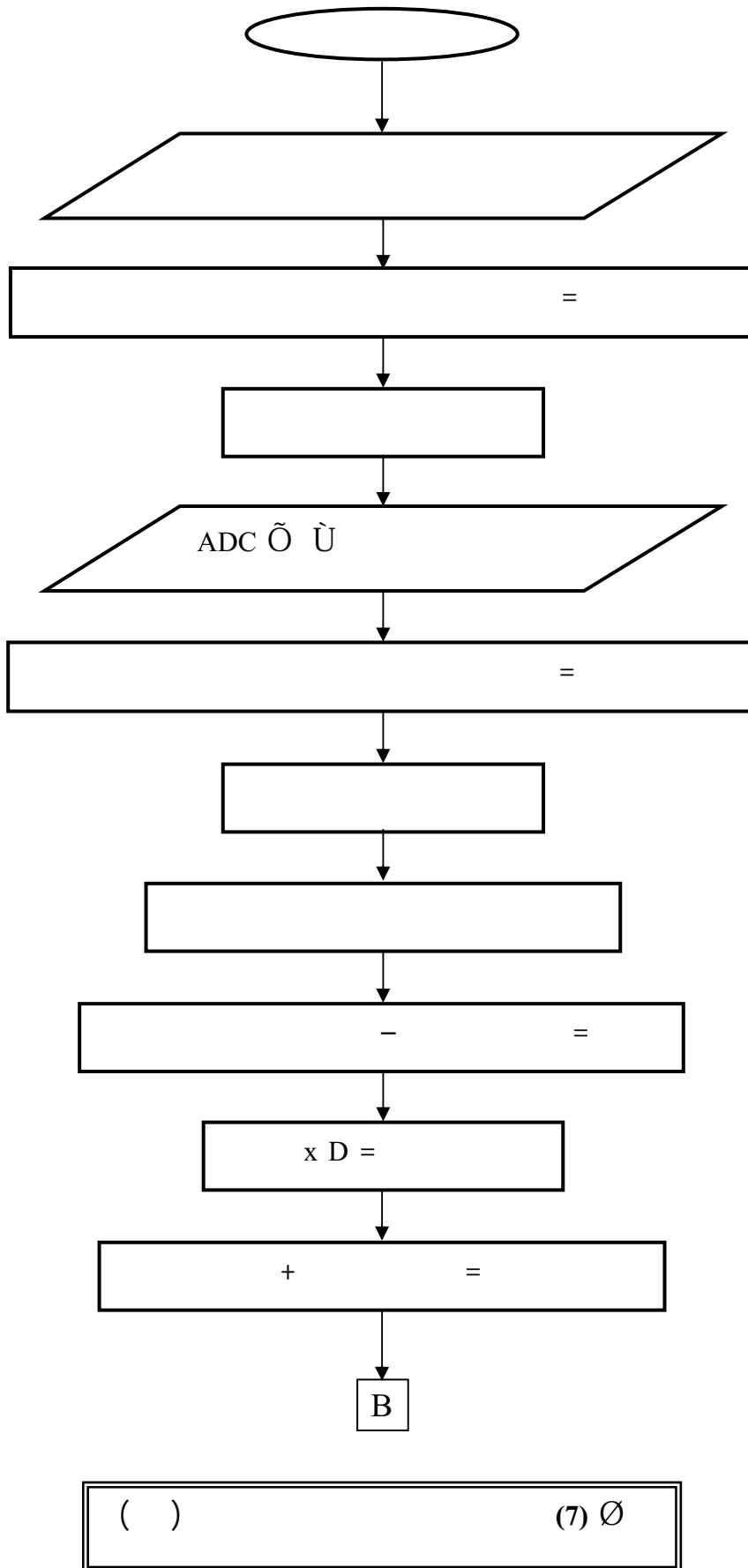


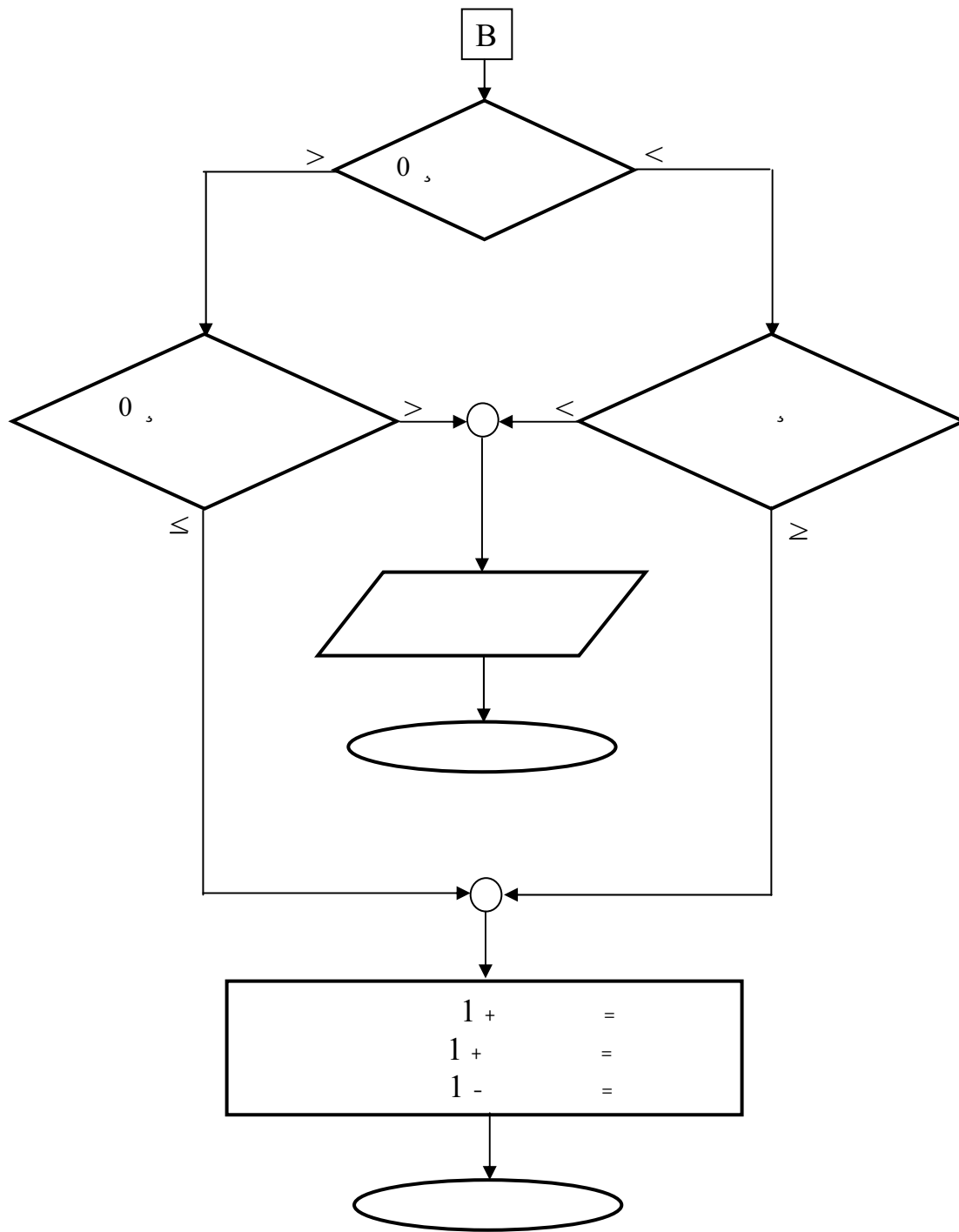
ISA slot ADC Õ (2) Û





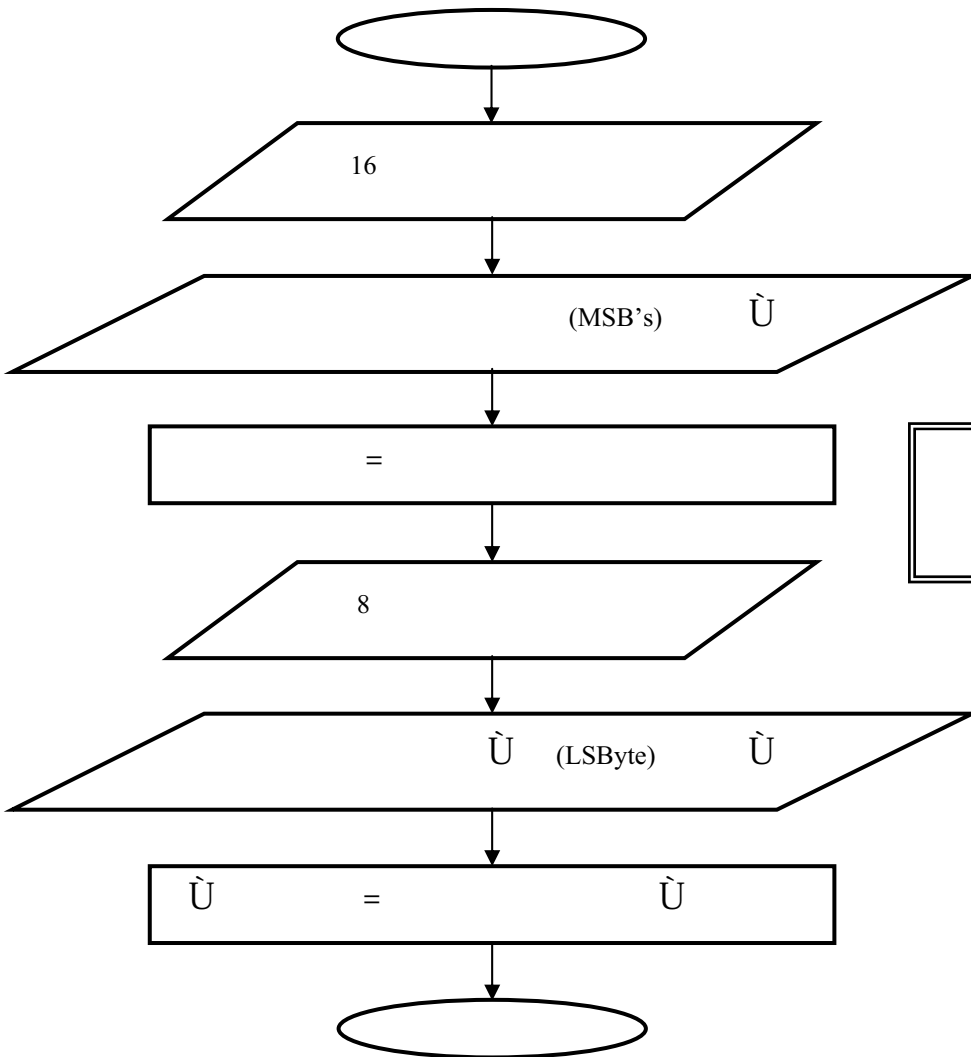
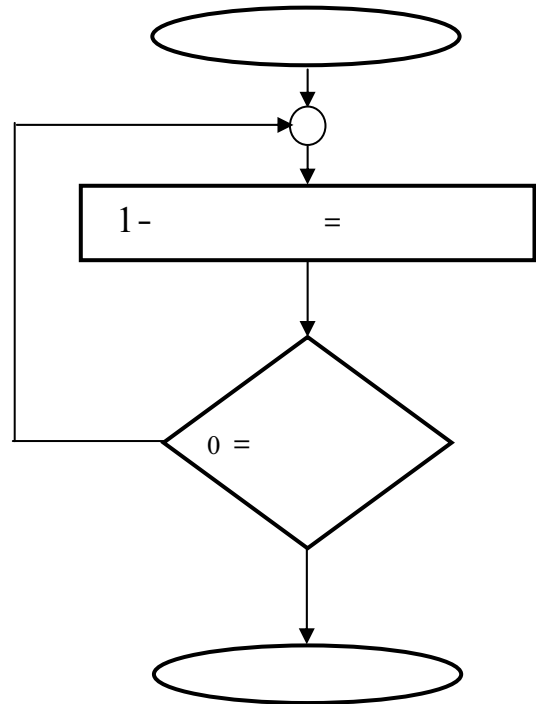




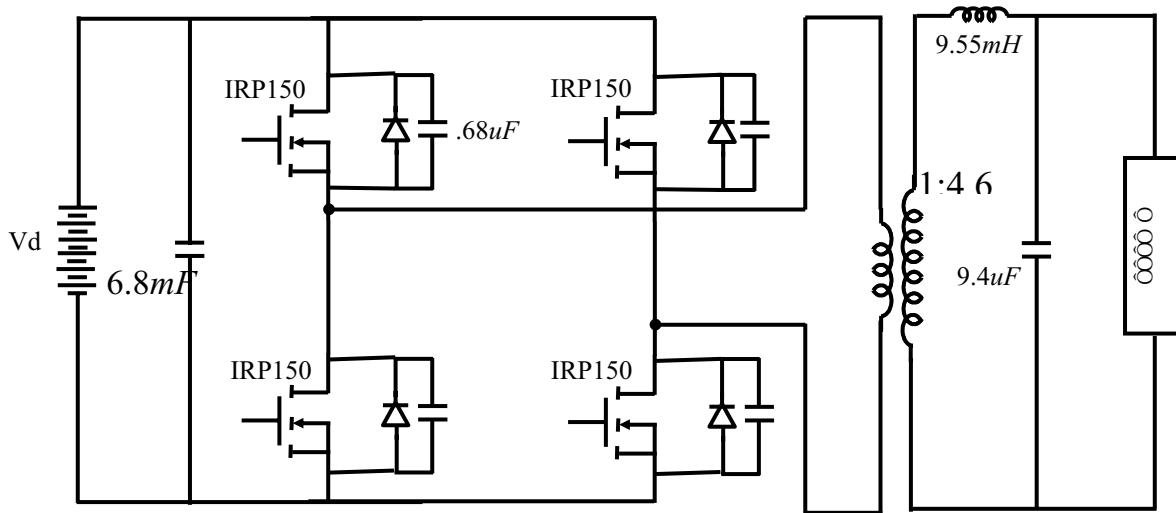


() (7) ∅

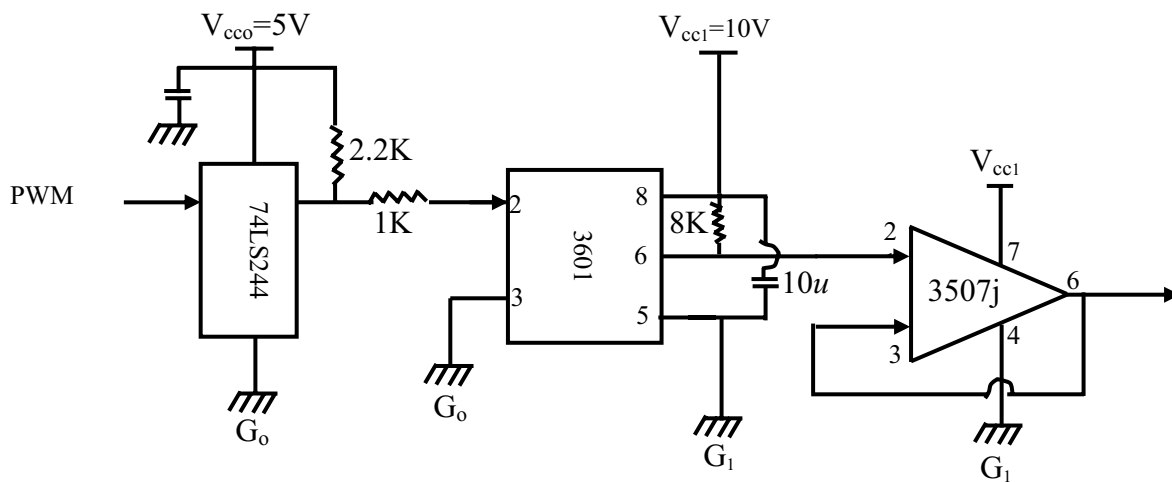
(8) Ø



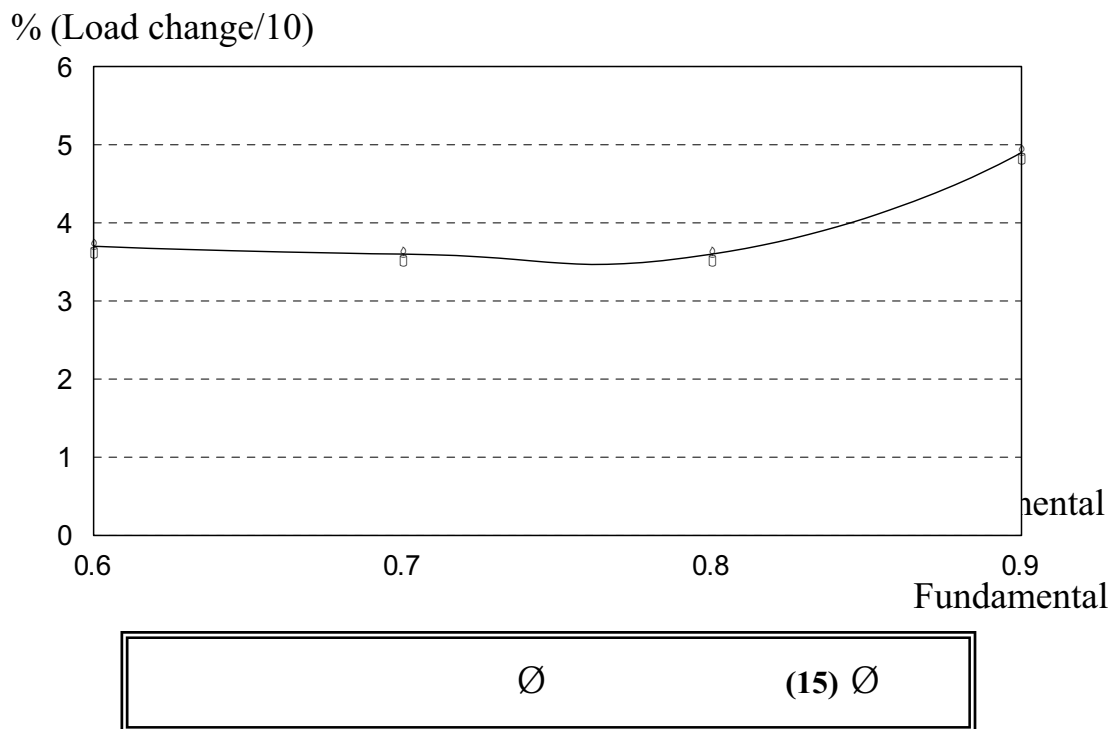
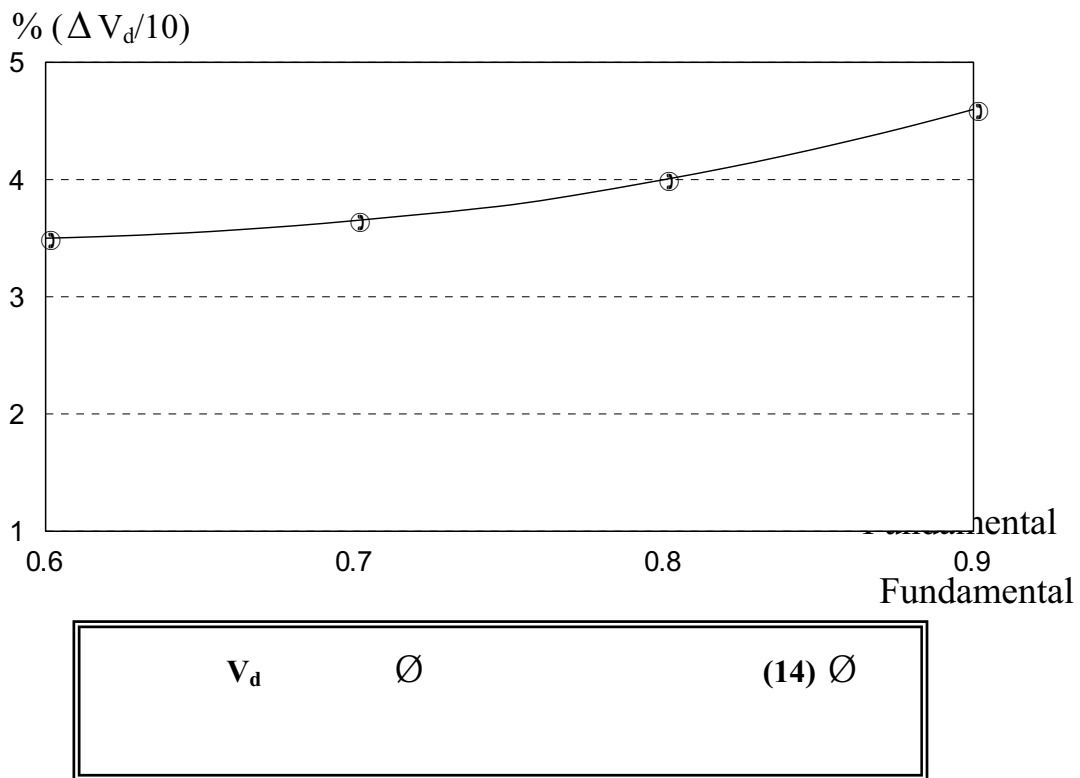
(9) Ø



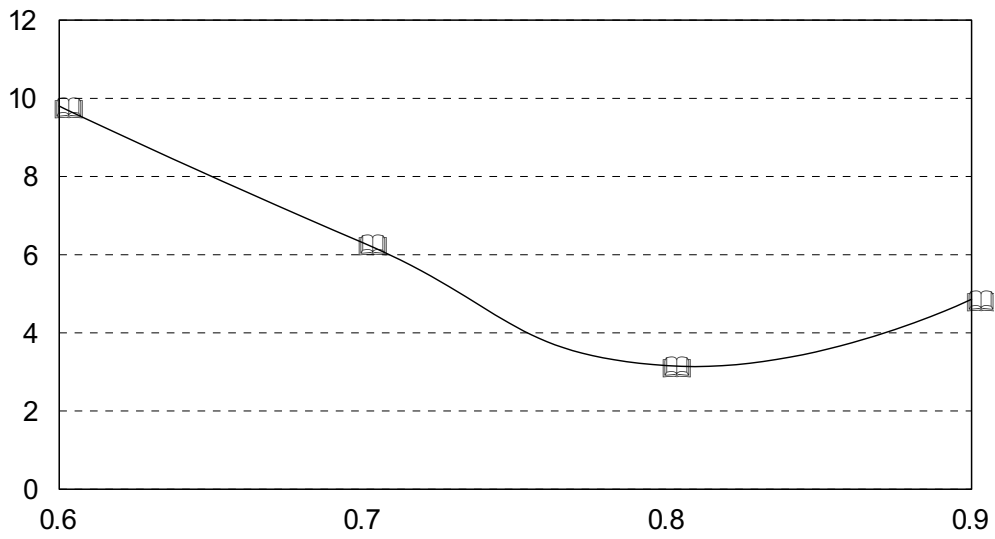
UPS $\hat{\circ}$ (10) \emptyset



MOSFET (11) \emptyset

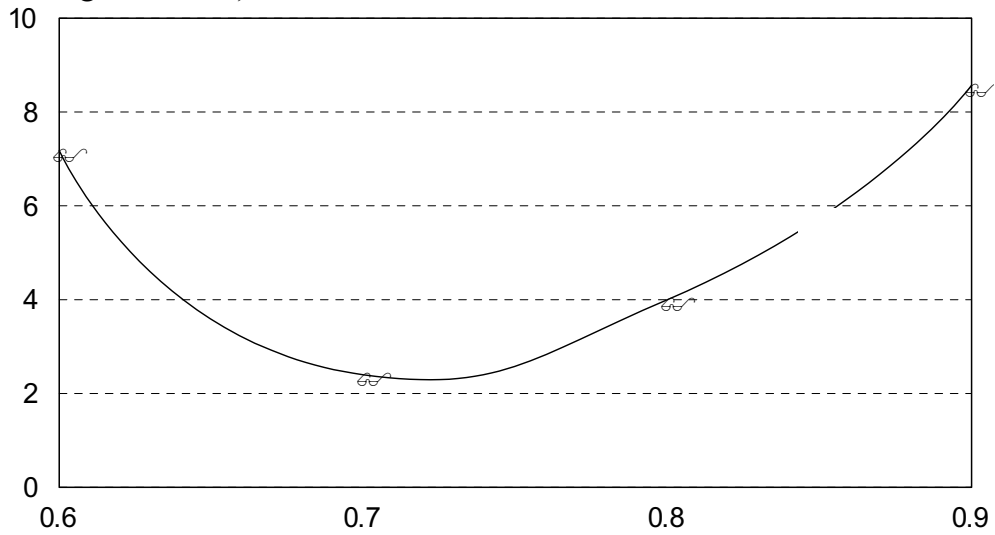


% (Load regulation/10)



∅ (12) ∅

% (Line regulation/10)



(13) ∅